# A 3D Photonic-Electronic Integrated Transponder Aggregator With 48 × 16 Heater Control Cells

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***Abstract*— An electronic integrated circuit (EIC) and a silicon photonic integrated circuit (PIC) are 3D-integrated. The EIC using the complementary metal–oxide–semiconductor (CMOS) part of STMicroelectronics' BCD8sp 0.16 $\mu$m technology controls all 768 switches in the PIC individually and monitors them with 84 transimpedance amplifiers. A scalable analog–digital approach with a cell size of 100 × 100 $\mu m^2$ for thermal control of optical ring resonator switch matrices is introduced. An electrical power consumption of 220 mW for all electronic control circuits of the optical switch matrix is resulting in 5.5% of the power needed by a constant-voltage control approach.**

***Index Terms*— Optical switches, micro-ring resonator, thermal tuning, 3D integration, electronic-photonic integration, low power consumption, heater control.**

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## I. Introduction

DUE to increasing data traffic demands, technological bottlenecks still present in current optical switching nodes of metro and core transport networks need to be removed in a cost-effective way in order to increase the transport resources utilization. Next-generation reconfigurable add- and drop-multiplexers (ROADMs) need to be provided with transponder aggregator switches (TPA) replacing the rigid port assignment of wavelength multiplexers and demultiplexers [1]. Although using photonic lightwave circuits (PLCs), commercial TPAs have been implemented [2], [3] and an architecture using a combination of spatial and planar optical circuits was presented [4], we believe silicon photonics is more cost-, size- and energy-efficient and performs better. A silicon-photonics-based TPA presented in [5] needs additional external tunable optical filters.

Our first results on the key test structures [6] motivated the development of a 48 × 16 switch matrix. The TPA presented here implements silicon nano-photonics and allows colorless (the add/drop switching structure is not color-specific), directionless (a wavelength can be added/dropped to/from any directions), and contentionless operation (adding/dropping in one direction does not produce contentions for other directions), working without external components. It has the highest level of scalability and miniaturization, being based on Si double micro-ring resonator (MR) switches [6]. It can be used either as an add or drop TPA, has four direction ports for reception or transmission towards the network and eight local ports for adding or dropping local wavelengths. Instead of the constant-voltage heater control approach of [6], a considerably power-dissipation-saving analog-digital heater control approach is demonstrated here.

## II. Architecture of the System

In Fig. 1 the architecture of the TPA is depicted. Fig. 1(a) depicts the main components in the photonic integrated circuit (PIC). In drop configuration, a comb of wavelengths received from the network is demultiplexed in two stages, first by interleavers second by array waveguide gratings (AWGs), prior to enter the optical crossbar matrix (48 × 16) of

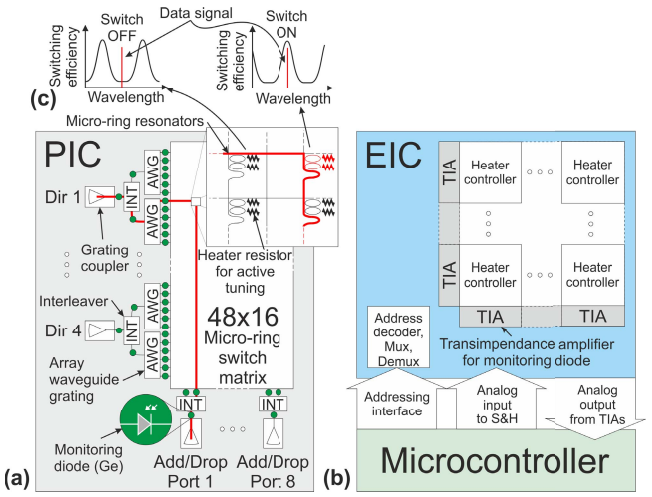


Fig. 1. Block diagram of the TPA. (a) Architecture of the photonic integrated circuit (PIC). (b) Architecture of the electronic integrated circuit (EIC). (c) Switching efficiency of the MR switching elements in OFF position (not heated) and ON position (heated) with respect to a data channel.

MR switch elements where the individual wavelengths are switched to the drop ports.

In add configuration, the wavelengths to be added to the network, connected to the add ports, are switched by the optical crossbar matrix to the proper output directions. Integrated Ge photodiodes in the PIC are used for monitoring.

Fig 1(b) shows an electronic integrated circuit (EIC) which tunes the photonic elements by individually heating them (824 heater control cells, 768 for MRs and 56 for interleavers and AWGs) and reads out the Ge diodes photocurrents through TIAs. Additional address decoders, analog multiplexer (MUX) and demultiplexer (DEMUX) blocks are used for interfacing.

The feedback system for calibration of the MRs is closed with an off-chip microcontroller. A comparison with commercial and new types of TPAs is presented in Table I.

## III. PIC Fabrication

Photonics wafers are fabricated in a fully complementary metal-oxide-semiconductor (CMOS)-compatible 8" fab with silicon-on-insulator (SOI) substrates featuring a 220nm silicon film on top of a 2$\mu$m thick buried oxide (BOX). The process flow allows to fabricate passive and active photonic devices such as Ge pin photodiodes, interleavers, wavelength multiplexers and MR switch elements, as well as devices with tuning capability using thermal heaters. 193nm lithography is used allowing minimum feature sizes of 120nm. The Back End Of Line consists of 1 Al-Cu interconnection level with W plugs and vias. An additional Under Bump Metallization process is done for 3D integration of electronics on photonics using copper micropillars [6]. Using micropillars instead of standard bond pads helps to reduce the final chip size and is crucial for potential scaling. The presented electronic-photonic integrated chip (EPIC) utilizes more than 2000 copper pillars. Using standard bond pads would considerably increase the chip size and impose long bond wires. Moreover, the increased parasitic capacitance would deteriorate the high-frequency performance of the pulse width modulation (PWM)

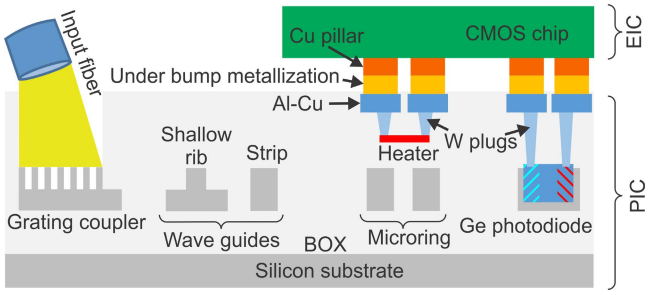


Fig. 2. Schematic cross section illustrating the 3D-integration (not to scale).

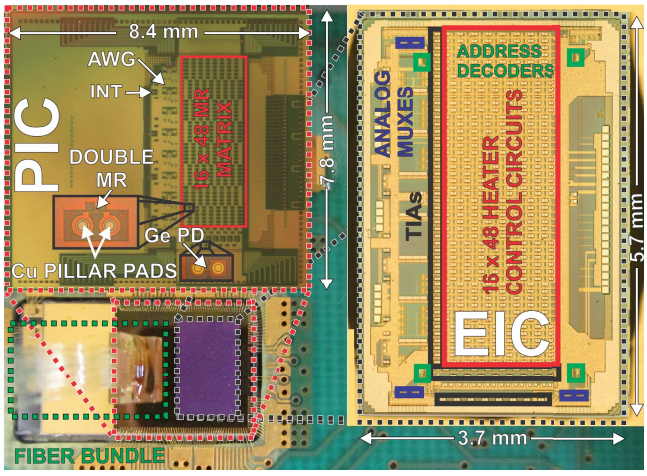


Fig. 3. EPIC wire-bonded to PCB inside the Al package with zoomed photos of PIC and EIC. The EIC is turned upside down. The chip area of the EIC is 21.1mm$^2$ while the chip area of the PIC is 65.5mm$^2$.

approach. Fig. 2 shows the schematic cross section of the 3D-integrated EPIC. In the complete module 99.27% of the heaters were working. The six non-working heaters can be explained by a few open micropillar connections. We expect that the yield of the micropillar connections will improve considerably in future.

## IV. Packaging

An aluminum package is used for the device assembly (board, TPA chip, Peltier cooler and fiber array) to allow for heat dissipation. A V-groove assembled fiber array was vertically coupled to the grating couplers. Fig. 3 shows a photo of the EPIC bonded to the printed circuit board (PCB) inside the Al package that also carries the microcontroller ATMEL XMEGA 128A1U, which contains 12-bit analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), of which we used 8 bits.

## V. Circuit Design

The analog-digital (hybrid) heater control circuit of a single cell is depicted in Fig. 4. An analog input voltage $V_{in}$ is stored in a sample-and-hold (S/H) circuit to set the heating power of the MR heater with digital PWM to minimize the circuit's power dissipation. PWM switching is provided by the operational amplifier (OPAMP) designed as a comparator. The chain of inverters at the output of the comparator enables fast switching of the N-channel metal-oxide-semiconductor

TABLE I
PERFORMANCE SUMMARY AND TPA COMPARISON WITH RECENT PUBLICATIONS

| | 8×8 Enablence TPA [2] | 8×8 Splitter-Switch TPA [3] | 8×24 SPOC TPA [4] | 8×8 Silicon Integrated TPA [5] | This work:4×8 Silicon Integrated TPA |
|---|---|---|---|---|---|
| **Architecture** | Multicast Switch | Multicast Switch | Wavelength Selective Switch (WSS)-type | Multicast Switch | Matrix of Microring Resonators (MR) |
| **Technology** | Planar Lightwave Circuits | Planar Lightwave Circuits | Spatial and Planar Optical Circuits | Silicon Photonics with thicker rib waveguides | Silicon Nano-Photonics |
| **Size (mm)** | 180×140×16 (packaged) | 110×15 | 72×28 (front end only) | 12×14 | 8.4×7.8 |
| **Loss (dB)** | 13.4 | 11.7 (average) | 16.2 (average) | 10.7-20.5 | ~14 |
| **Response Time (μs)** | 6000 | Tens ms range (not reported) | Tens ms range (not reported) | 20 | 4 |
| **Crosstalk (dB)** | -40 (Switch only) | -40 (Switch only) | -20.5 | -35 (Switch only) | -35 |
| **Polarization dependent loss (dB)** | 0.4 | Low (not reported) | Low (not reported) | 0.6 | Single polarization, (Transverse electric) |
| **Notes** | Needs tunable filters | Needs tunable filters | Integrated front end assembled with free space optics components | Needs tunable filters | |

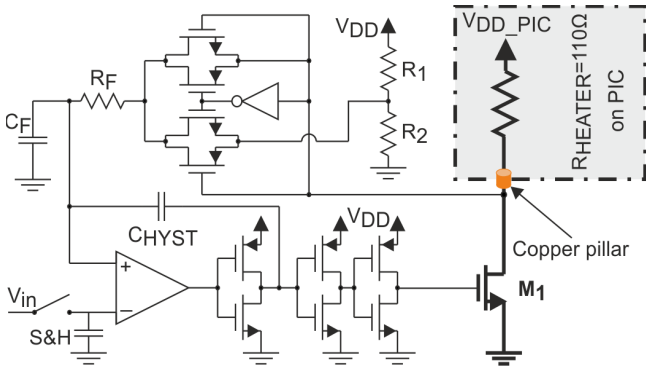


Fig. 4. Schematic of analog-digital (hybrid) heater control cell consisting of analog-to-PWM converter.

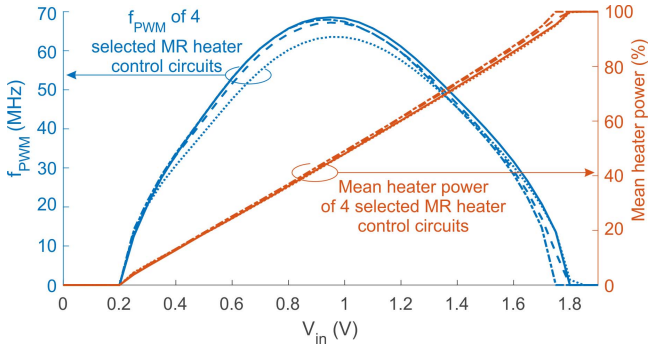


Fig. 5. Characteristics of heater power (right axis) and PWM frequency (left axis) in dependence on input voltage $V_{in}$ (Duty cycle of PWM signal is proportional to $V_{in}$).

field-effect transistor (MOSFET) M1 (rise/fall time≈250ps). The switching frequency range is determined by the feedback filter consisting of $R_F$ (200kΩ), $C_F$ (210fF) and $C_{HYST}$ (25fF). The circuit's layout with a $15 \times 15 \mu m^2$ copper pillar pad fits into the matrix cell of $100 \times 100 \mu m^2$.

## VI. EIC CHARACTERISTICS

The measurement results of the mean heater power and PWM switching frequency versus $V_{in}$ for 4 selected switching cells are shown in Fig. 5. A major improvement of this circuit compared to the circuit described in [7], where only 16 cells were present, is that the maximum heater power is now reached for $V_{in} = 1.8V$ instead of 0V. This is important, because without refresh the S/H's leakage current discharges the hold capacitor over time. The start of the characteristics in Fig. 5 at ~0.2V is intentional to guarantee that all heaters can be turned off also in the case of worst-case OPAMP offset voltages. Mismatch of the characteristics can be handled by calibration, which is done for the photonic components anyway.

In Fig. 5 the PWM frequency versus $V_{in}$ is shown for 4 selected matrix cells. The PWM frequency depends on $V_{in}$ and reaches its maximum approximately at 50% heater power. The maximum PWM frequency is about 70MHz, which is much higher than the PWM frequency of a purely digital 7-bit heater control cell of 7.58MHz [8], and therefore reduces the PWM-induced temperature ripples considerably compared to [8]. At VDD = 1.8V, room temperature and maximum switching frequency, power consumption of the comparator is ~77$\mu$W, while the driver for MOSFET M1 consumes ~131$\mu$W, resulting in a total power consumption of ~208$\mu$W per heater driver. This is almost 90% less than the power consumption of the heater driver used in [9], which additionally has a smaller maximum heater power of 12.25 mW, compared to the ~29mW of the heater resistor presented within this work.

## VII. EPIC CHARACTERISTICS

Fig. 6 shows the switch working when one channel is added to direction 4 for two different scenarios (switch A active or switch B active) for switching either an odd or an even channel. It reports the transmission spectra at the different stages within the device. A tunable laser (6 dBm) was injected into the input fiber, while the transmission at the output was recorded with an InGaAs detector. Fig. 6(a) shows the signal paths within the chip. Fig. 6(b) shows the fiber to fiber insertion loss, i.e. the measured transmitted signal at the output with respect to the input signal. We note two transmission peaks due to the selection of the odd or even channel by one of the switches (A or B) of the switch matrix. A total insertion loss of about −22dB, a 1-dB channel bandwidth of 60GHz and a 3-dB channel bandwidth of 100GHz, and a channel isolation of better than −35dB, were measured. Figs. 6(c)-(e) show the in-the-chip spectra measured by the monitor Ge photodiodes

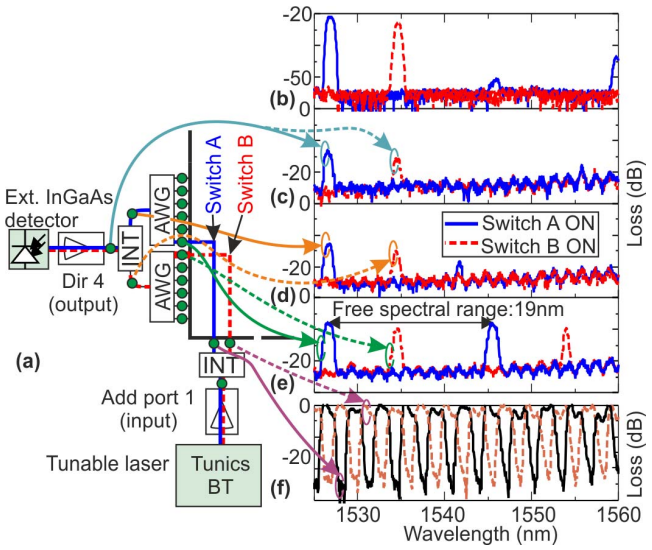


Fig. 6. Measured performance of the electronic-photonic integrated chip in add configuration for two aligned switch nodes (switch A and switch B). The system was kept at 38.8°C by means of a dedicated Peltier cooler. Interleavers and AWGs were aligned by means of dedicated heaters. (a) Signal paths within the chip. (b) Total insertion loss from input to output. (c)-(e) In-the-chip spectra after the interleaver at the direction port (c), after the AWGs (d), and before the AGWs (e). (f) Interleaver transmission at the add port. The interleaver transmission (f) does not depend on the switches.

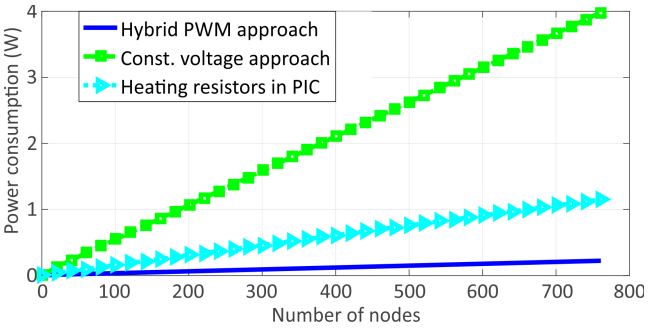


Fig. 7. Comparison of power consumption.

at the interleaver output, and at the AWG output and input, respectively, normalized to the signal from the first photodiode after the input grating coupler. Fig. 6(f) shows the interleaver transmission demonstrating the splitting of the input signal into even and odd channels (almost 0dB device losses on the channels and more than 25dB of channel isolation). A free spectral range of 19nm and an overall on-chip device loss of $\sim -14$dB was measured ($\sim -5$dB from the AWGs, and $\sim -9$dB from the rings, the waveguides and the waveguide crossings), which results in a total insertion loss of $\sim -22$dB including the loss of the input/output gratings couplers ($\sim -4$dB per coupler). We believe that the total insertion loss can be reduced by improving the designs of the grating couplers and the AWGs and by a better fabrication of the waveguide crossings.

Since in the typical operation of the switch matrix only a few MRs are on, power consumption for driving them can be neglected in an analysis of the total power consumption of the full matrix, in our case of 768 switching nodes.

For compensation of process tolerances of the MRs each of the off-MRs needs to be driven in average by typically 1.5mW. In Fig. 7, a comparison of the power consumption of EICs with different approaches for driving MR heaters as a function of the number of optical switches in the matrix is shown. Compared are control EIC circuits with a constant-voltage approach, the proposed hybrid approach and the power dissipated by the heaters inside the photonic IC.

## VIII. Conclusion

For the presented 768-node switching matrix, all circuits of hybrid heating control inside the EIC dissipate 220mW. The total heating power of heaters inside the PIC is 1.15W. The power dissipated in the EIC by applying a constant-voltage heating control is estimated to 4W. The ratio between the power consumption of the proposed hybrid and the constant-voltage approach is 5.5%. Compared to [8], the PWM resolution was increased from 7 to 8 bits and the maximum PWM frequency was increased by a factor of more than 8.

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